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	Subclass
Class	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

I.P.E.	PATENT DATE
SCANNED 4 Q.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/802664	D	~~257~~ 438	773	~~2818~~ 2823	~~AUDUSAR~~ H. LEE

APPLICANTS: Rajendra Pandey

TITLE: Flip chip interconnection structure

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			Continued on label on inside file jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to (date) has been disclaimed.	(Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S. Patent No.	(Primary Examiner) (Date)			ISSUE FEE	
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